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Package Design Improvement for Wire Shorting Resolution

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

New devices and new technologies in semiconductor industry are getting more complex in terms of package layout, direct materials, and process capability. With the package design complexity, several issues are encountered during the development, and in turn affecting the overall yield of the package. The paper discusses the modification and improvement done on the bond/lead finger where the wire has issues on shorting with the soldermask during wirebonding process. With the design improvement, occurrence of wire shorting to soldermask would be mitigated.

Keywords: Substrate; wire short; soldermask; package design.

1. INTRODUCTION

The process of attaching wire to a bond pad and lead finger is called wire bonding process. This process is one challenging process in semiconductor industry especially in assembling an integrated circuit (IC), responsible in attaching or bonding wires to provide electrical connections through combination of heat, pressure and thermosonic energy. With the design of new

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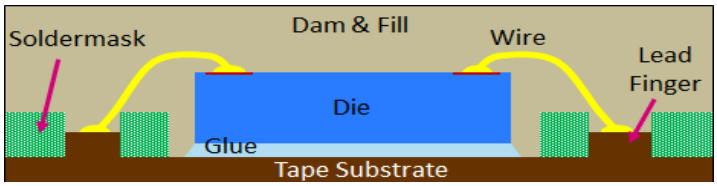

Fig. 1. Cross-sectional view of micromodule package

technologies in the semiconductor manufacturing, a huge challenge exists particularly shown in Fig. 1 wherein the wires are almost touching the periphery of the soldermask inside the micromodule device. This paper presents a solution to successfully process this type of technology in the semiconductor industry market by modifying the substrate design through augmenting the lead finger configuration.

Parametric adjustment also done on this study to see if there is another solution to eliminate wire touching the soldermask, unfortunately the defect is still occurring. The direct materials used in this package are, silicon die, epoxy or adhesive tape substrate, and Gold (Au) wire. A silicon die is a small block of semiconducting material on which a given functional circuit is fabricated. Typically, integrated circuits are produced in large batches on a single wafer of electronic-grade silicon (EGS) or other semiconductor (such as GaAs) through processes such as photolithography. The wafer is cut (diced) into many pieces, each containing one copy of the circuit. Epoxy or glue serve as an adhesion of the silicon die to glued and not easily break whether conductive and non-conductive glues. A substrate material provides the surface on which something is deposited or inscribed, for example the silicon wafer used to manufacture ICs [1]. A wire is used to provide electrical connections between the silicon dies and the lead finger of the semiconductor device using very fine bonding wires. The wire used in wirebonding process is usually made either of Gold, Copper (Cu), or Silver (Ag) [2]. To guarantee its integrity during production run, wirebond process is incorporated with a multiple of criteria such as third optical inspection or visual inspection, ball size, ball height, ball aspect ratio (BAR), wire pull test, ball shear test, stitch pull test, loop height, intermetallic compound (IMC) and contact angle. The wirebond criteria is performed after machine conversion or set-up to ensure that the product is reliable when subjected to a reliability test.

2. ASSEMBLY PROCESS FLOW

Given in Fig. 2 is the assembly process flow of micromodule packages. Worthy to note that assembly manufacturing processes vary with the technology and the product [3-5]. For this device, the wafer is prepared prior grinding, and afterwards be grinded on the bottom part with the required die thickness of the wafer. Next process is laser grooving wherein the silicon dies is cut into half. Another meaning of laser grooving is a thermal energy based process and there is no direct tool-to-work piece contact. It uses a focused high-energy laser to transfer thermal energy to the wafer, which is absorbed by the topmost low thermal energy ILD metal layers [6-8]. These metal layers then heat up and melt into molten and vaporized solids, which can be removed by directional flow of air pressure. Automatic optical inspection is type of machine that serve as an eye to inspect the wafer after laser groove process afterwards, the dies will cut into pieces with the desired die sizes and this process called wafer sawing. Next process is the die attach wherein it is responsible in picking the silicon die to place it on the tape substrate and with a snap cure machine to cure the unit immediately. Next process is wirebonding serve to provide electrical connections into silicon dies and lead finger of the substrate. After wirebonding is potting process, this process where the units are encapsulated with dam

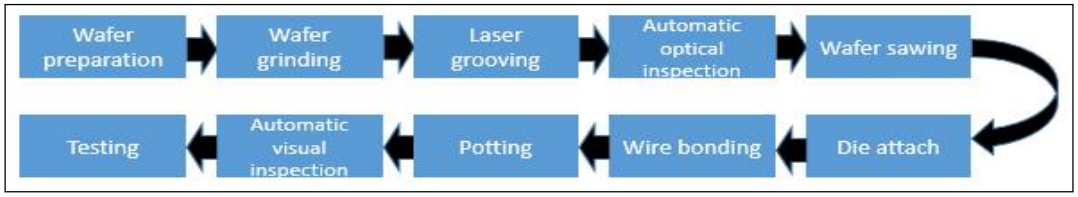

Fig. 2. Micromodule assembly process flow

and fill. Next process is automatic visual inspection to see if there is any defect after the process of potting and the last process is testing, this process wherein the units will undergo testing before shipping to our customers.

3. PROBLEM IDENTIFICATION

During the development phase of the product, one of the top assembly rejects is the wire touching or shorting with the soldermask as highlighted in Fig. 3. This is mainly because of the respect to the top surface of the soldermask. More importantly, the reject is manifested during wirebonding process. This reject manifestation will eventually fail during the reliability of the product. By the growing demand in the market for this product, indeed this is a very big challenge especially during the package development phase.

4. DESIGN SOLUTION AND DISCUSSION OF RESULT

An augmented and improved semiconductor substrate design is presented in Fig. 4. wherein the bond finger or lead finger is coplanar or leveled with the soldermask surface. The improved substrate design will eliminate the occurrence of the top assembly reject during the assembly manufacturing of the product. Furthermore, the design will also result to better reliability of the product.

With the data shown in Fig. 5, the new substrate design significantly improved and eliminated the occurrence of wire touching the solder mask with 78 percent improvement in parts per million (PPM) level. Note that actual values are intentionally not shown. Also, criteria for rejects are governed by assembly design rules and work instructions [2,9-10].

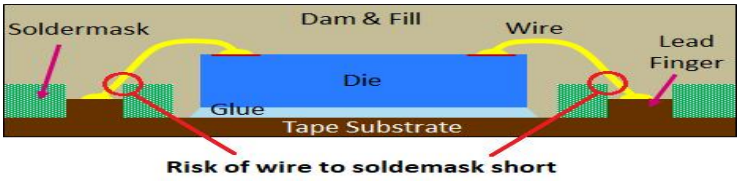

Fig. 3. Defect of wire shorting to soldermask

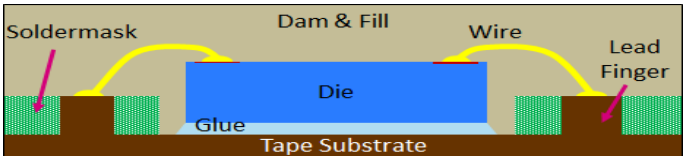

Fig. 4. Substrate design improvement with augmented lead finger configuration

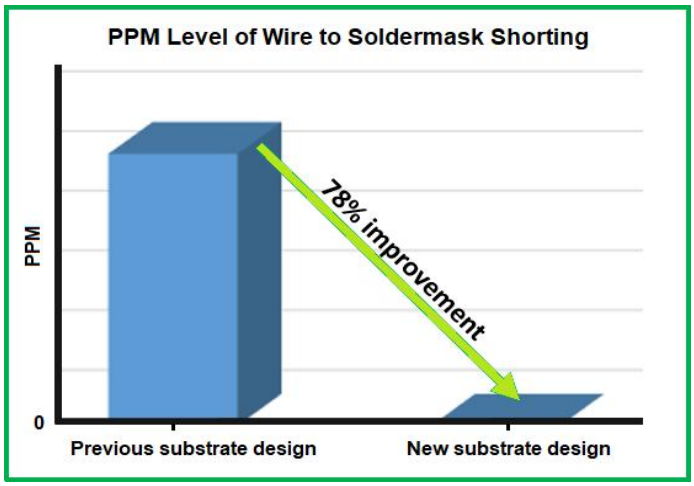

Fig. 5. PPM level performance for the defect of wire touching the soldermask

5. CONCLUSION AND RECOMMENDATIONS

The paper presented a process solution and improvement with the improved substrate design, which significantly resolved the assembly reject occurrence of wire touching the soldermask during wire bonding process. The new substrate design offered a better bondability and provided a good reliability as well. Worth noting is that continuous process and design improvement is really important to foster and sustain high quality performance of semiconductor products and its assembly manufacturing. Studies in [6-8,11-12] are helpful in reinforcing robustness and optimization of assembly processes.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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