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Investigation on Die Crack in a Stacked Die Package Using Finite Element Analysis

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Author's contribution

The sole author designed, analysed, interpreted and prepared the manuscript.

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ABSTRACT

Die crack is one of the problems in stacked die semiconductor packages. As silicon dies become thinner in such packages due to miniaturization requirement, the tendency to have die crack increases. This study presents the investigation done on a die crack issue in a stacked die package using finite element analysis (FEA). The die stress induced during the package assembly processes from die attach to package strip reflow was analyzed and compared with the actual die crack failure in terms of the location of maximum die stress at unit level as well as strip level. Stresses in the die due to coefficient of thermal expansion (CTE) mismatch of the package component materials and mechanical bending of the package in strip format were taken into consideration. Comparison of the die stress with actual die crack pointed to strip bending as the cause of the problem and not CTE mismatch. It was found that the die crack was not due to the thermal processes involved during package assembly. This study showed that analyzing die stress using FEA could help identify the root cause of a die crack problem during the stacked die package assembly and manufacturing as crack occurs at locations of maximum stress. The die crack mechanism can also be understood through FEA simulation and such understanding is very important in coming up with robust solution.

Keywords: Die crack; stacked die; die strength; thin die; finite element analysis.

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1. INTRODUCTION

With semiconductor package miniaturization and increased functionality requirements, thinner silicon dies are stacked in a single package. However, thinner die has higher potential to have severe crack as compared to the larger one at die attach process [1]. Although not often taken into consideration, higher dynamic impact force at die attach also causes die crack [2]. Wafer handling and transport is also another process step that induces mechanical stresses in the wafer specifically due to wafer deformation with Bernoulli gripper [3]. During wafer sawing, monocrystalline silicon being a hard and brittle material, is extremely prone to edge chipping that also contributes to die crack problem. The edge chipping size can be reduced by using ultrasonic assisted sawing demonstrated that different sawing processes present different material removal modes and edge quality [4]. Different modes of die cracking were seen in high end flip chip applications. It was mentioned that defects induced during the dicing process cause horizontal die cracking. Vertical crack under thermal loading is a result of surface defects on the back side of the die which may have been introduced as back side etches. Reduction in back side defects, dicing defects, and CTE mismatch could help eliminate die crack problem [5]. Lower die mechanical strength due to defects could be one contributing factor to the die crack issue [6].

Finding and understanding the factors involved in a die crack is very important for the root cause investigation. Identification of the true root cause allows the implementation of accurate solutions. In the current study, die crack was encountered in a stacked die package. The actual die crack is shown in Fig. 1. The package has two stacked dies with the thinner bottom die bonded to the substrate using die attach film (DAF) adhesive. The crack was observed in the thinner bottom die. The film over wire (FOW) that is used to bond the second die over the bottom die also shows a crack. Fig. 2 shows the location of the units with crack mapped within the substrate strip. It can be observed that most of the units with die crack are located towards the center of the strip. An investigation on this specific die crack problem was done using finite element analysis (FEA) technique to analyze die stress induced during the package assembly processes like die attach, molding and package reflow as well as the strip handling or bending.

2. PACKAGE DIE STRESS ANALYSIS

Finite element analysis (FEA) technique is very useful in conducting die stress analysis. This was used in previous studies [7,8] to analyze the effect of varying geometric parameters like die size and thickness, and the die attach materials with different modulus. The effect of dice design, temperature, or mechanical properties of the materials on crack thresholds was investigated using this stress modeling technique [9]. FEA was also used in the study of cleavage fracture of brittle semiconductors with samples under specific loading conditions [10]. This FEA approach has now been used in studies on stacked overhang die during wire bonding [11], underfill fillet cracks [12], die edge crack propagation [13], impact of die attach film (DAF) modulus on thin die crack issue [14] as well as on the comprehensive optimization to eliminate die crack in a leadframe-based package [15].

In this study, a strip FEA model was created and analyzed using ANSYS simulation software. The model, as shown in Fig. 3, considers the substrate with die 1 (bottom die bonded) after die attach 1. Another model takes the condition after die attach 2 in which the top die is stacked above the thinner bottom die (die 1). The thickness of the bottom die is 70 microns, which is much thinner compared to the top die that has a thickness of 420 microns. The third model is for the stacked die already encapsulated with epoxy molding material. The encapsulated package or molded strip model includes the substrate, DAF, bottom die, FOW, top die and the epoxy molding compound. Corresponding material properties like modulus, coefficient of thermal expansion (CTE) and Poisson's ratio were assigned to each package component.

Die stress analysis in this study considers the package assembly processes involved in producing the stacked die package described. In the first set of die stress analysis, the stress in the bottom die (die 1) after DAF or die attach cure (die attach 1) was simulated and maximum stress location identified. This is a thermally induced stress in the die due to CTE mismatch of the substrate, DAF and die. The stress-free temperature was set at a value equal to the curing temperature of the specific DAF material used. The bending of the strip due to handling was also simulated to get the mechanical stress in the bottom die and analyze its maximum location at unit level and strip level. Then the second set of analysis was considering the die stress after the bonding of the top die on the

thinner bottom die and the curing of the FOW adhesive (die attach 2). With the substrate having the two bonded stacked dies, mechanical stress due to strip bending was also analyzed. The third set of analysis was on the molded strip after post mold cure (PMC) at 175°C and during package strip reflow at 260°C. Stress induced in the die due to bending of the molded strip was also simulated.

3. RESULTS AND DISCUSSION

The result of the stress in the bottom die after DAF curing is shown in Fig. 4. At strip level, die stress is almost the same for all the units within the strip. High die stress areas are uniformly distributed within the strip. It is also observed that there is a "frowning" strip warpage after die attach curing. At unit level, the maximum die stress is at the center of the die, top surface as shown.

Die stress due to strip bending is shown in Fig. 5. It indicates that high die stress areas are concentrated towards the center of the strip. At unit level, the maximum die stress location is parallel to the Y-axis, top surface as shown. As indicated, Y-axis is parallel to the short side of the whole substrate strip. The maximum die stress location is at some distance from the die edge but not also exactly at the centerline of the die. This bending stress distribution is completely different compared to the stress induced due to CTE mismatch after DAF curing.

The result of the second set of simulation after FOW adhesive curing (die attach 2) is shown in Fig. 6. With the thicker top die already bonded on top of the bottom die, the maximum die stress is still observed in the bottom die. The maximum stress in the top die is lower compared to the stress in the bottom die. This shows that the thinner die is more prone to die crack than the thicker die in this specific stacked die package. However, the location of the maximum stress is now in a different direction, which is parallel to the long side of the whole substrate strip as shown in the unit level die stress contour plot (Fig. 6). At strip level, the high die stress areas are also uniformly distributed within the strip and there is some reduction in the frowning warpage as there are now two stacked dies on the substrate strip.

Die stress result under strip bending with two stacked dies already bonded is shown in Fig. 7. The result at strip level shows that the high die stress areas are concentrated towards the center of the strip. The unit level result has the maximum die stress parallel to the short side of the whole strip. This is similar with the direction of maximum die stress of the substrate having only the bottom die bonded and subjected to strip bending (Fig. 5).

For the molded strip, die stress results after post mold cure (PMC) and during package strip reflow are shown in Fig. 8. The results at strip level show that the high die stress areas are uniformly distributed within the whole strip for both simulated conditions. At unit level, the location of maximum die stress is parallel to the long side of the whole strip or the X-axis as indicated. After PMC, the maximum die stress is along the die edge. During reflow, the maximum die stress is at some distance from the die edge.

With strip bending of the molded strip simulated, the die stress result is shown in Fig. 9. At strip level, the high die stress areas are concentrated also towards the center of the whole strip. However, at unit level the location of maximum die stress is at the die edge of the thinner bottom die.

With the maximum die stress location identified using finite element analysis, determination of the possible cause of the die crack problem encountered and the mechanism of failure could now be done. Results from die stress analysis show that the die crack encountered is more of a mechanically induced stress or stress due strip bending rather than a thermally induced stress due to CTE mismatch of the package component materials.

At strip level, actual locations of units with die crack are generally concentrated towards the center of the strip (Fig. 2). This matches with the location of high die stress areas under substrate strip bending, which is concentrated towards the center of the simulated strip. The unit level results under strip bending with maximum die stress parallel to the short side of the substrate strip are also in agreement with the actual crack orientation (Fig. 1). This strip bending could be due to strip handling issue during package assembly and other conditions in the manufacturing setup that would create substrate bending.

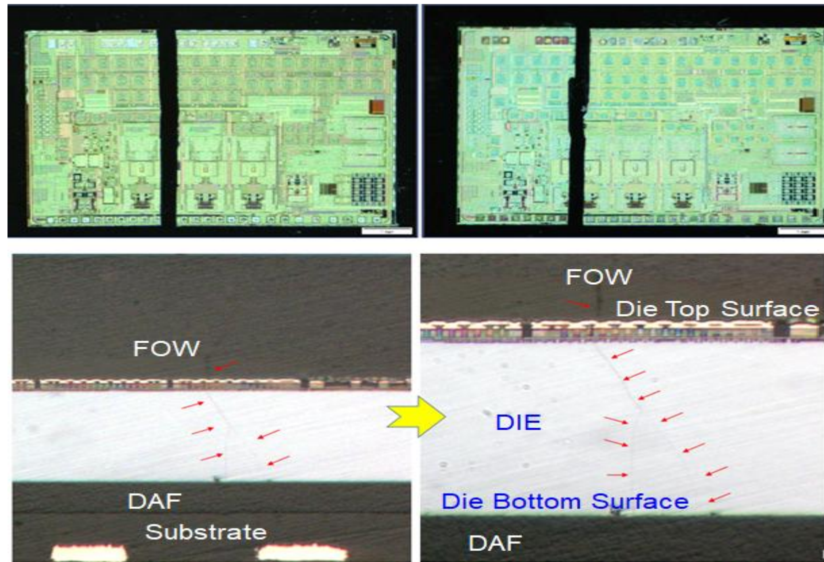

Fig. 1. Die crack encountered with the thinner die in a stacked die package

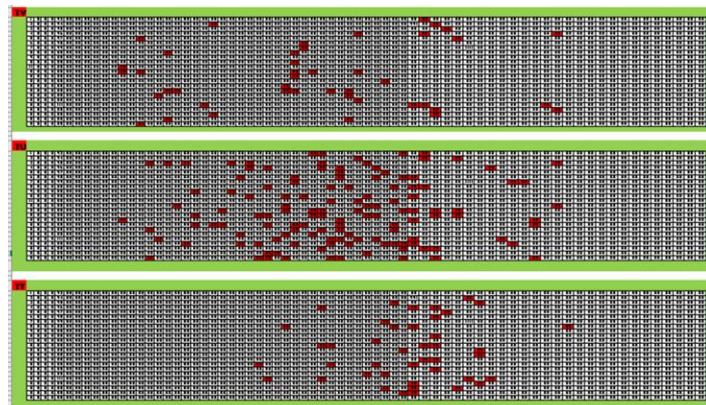

Fig. 2. Location of the units having die crack with respect to the substrate strip

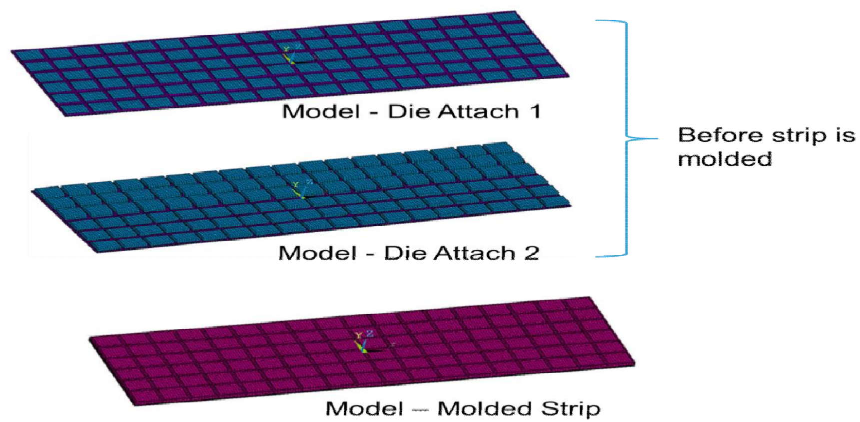

Fig. 3. Finite element analysis (FEA) model of the stacked die package strip

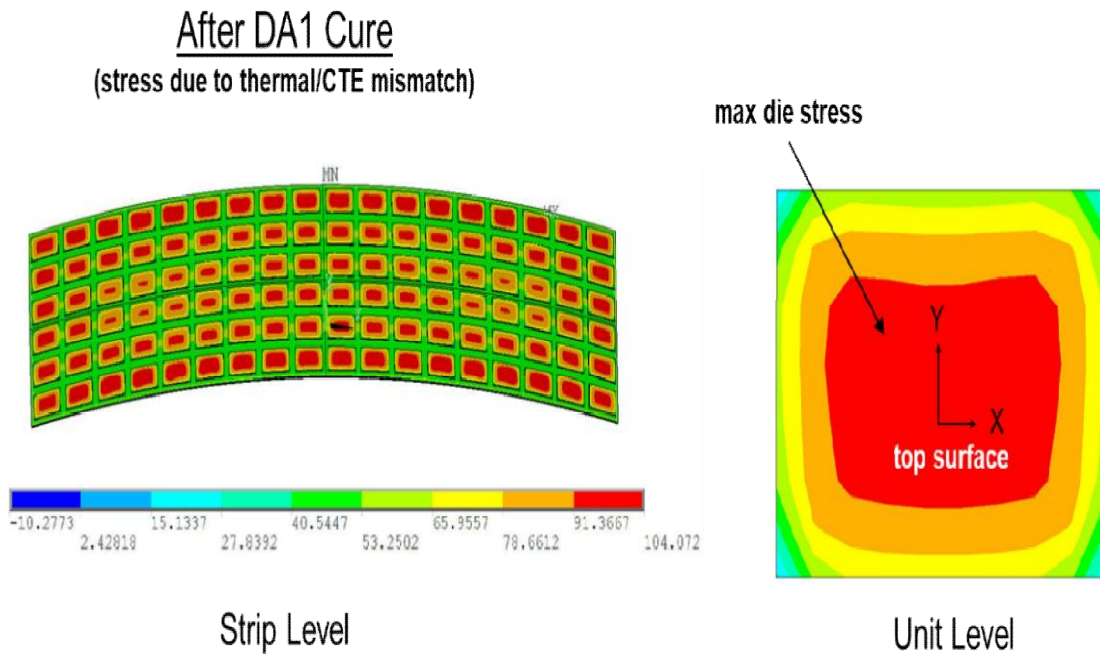

Fig. 4. Die stress result after die attach cure (die attach 1)

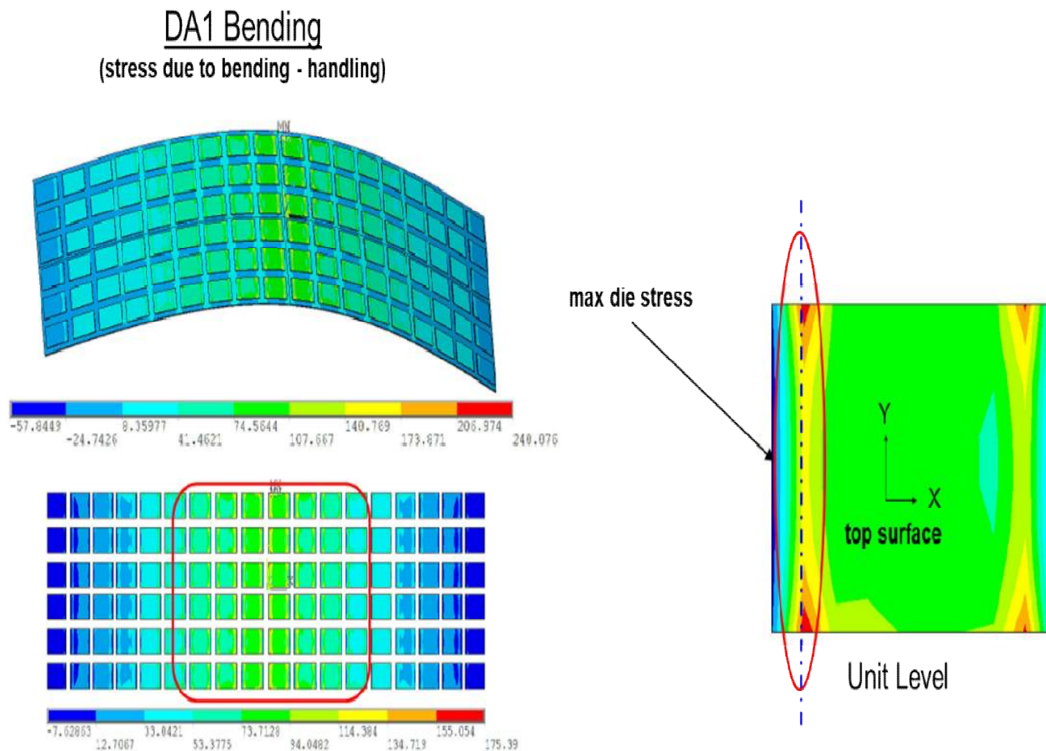

Fig. 5. Die stress result under strip bending with die 1 already bonded on the strip

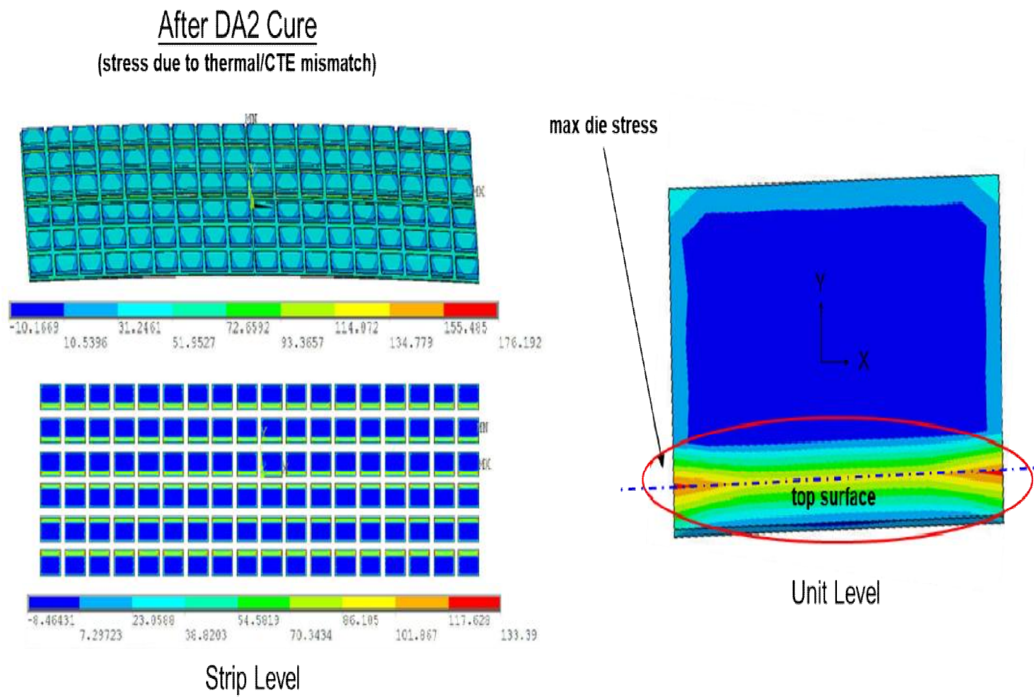

Fig. 6. Die stress result after die attach cure (die attach 2)

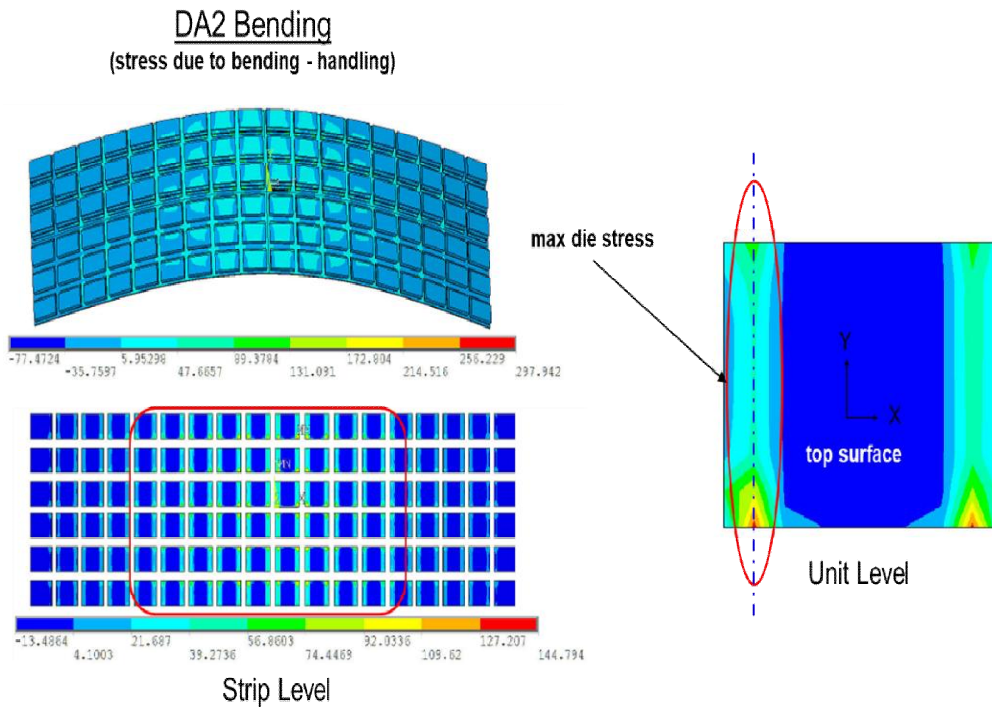

Fig. 7. Die stress result under strip bending with die 1 & die 2 already bonded on the strip

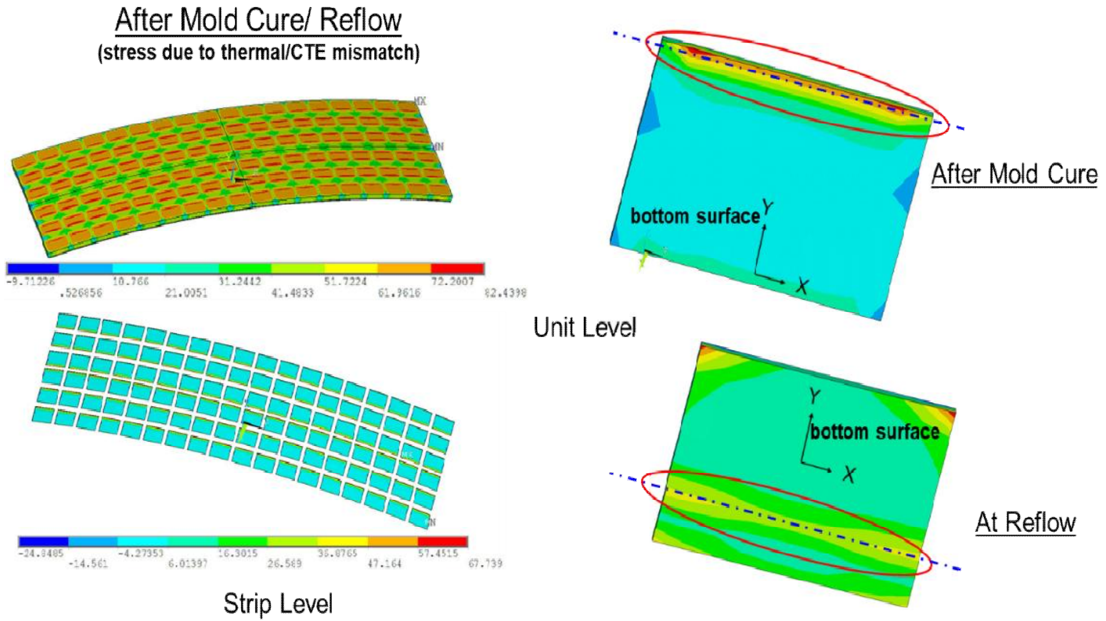

Fig. 8. Die stress result after post mold cure and during package strip reflow

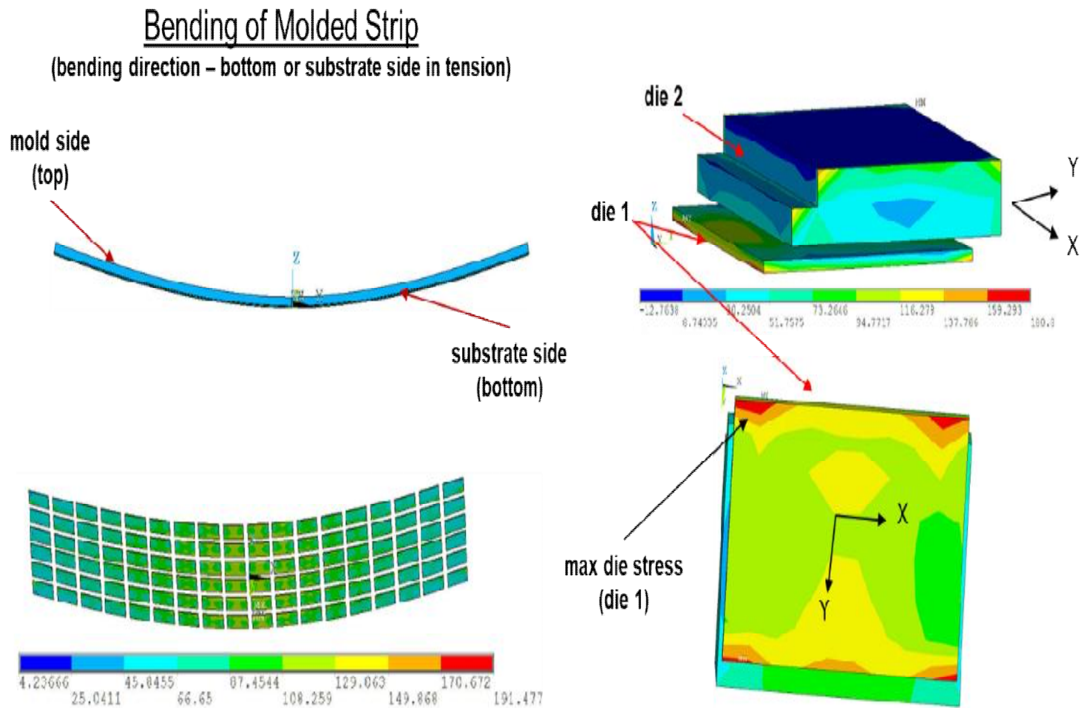

Fig. 9. Die stress result under molded strip bending

4. CONCLUSION

It is concluded that finite element analysis (FEA) is a very useful technique for investigating die crack in a stacked die package and even in other semiconductor packages. Determining the location of maximum die stress at strip level and unit level can help in matching the actual die crack with the process or condition that is the most likely cause of the crack. The die crack mechanism can also be understood through die stress analysis using FEA. In the current study, the die crack problem was attributed to strip bending (mechanically induced) and not due to the CTE mismatch of the different package materials (thermally induced).

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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COMPETING INTERESTS

Author has declared that no competing interests exist.

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