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Implementation of Pads Re-layout for QFN Multi-row Breakthrough

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

An alternative design of Quad-Flat No-lead (QFN) leadframe capable with three or more arrays of lead is discussed and presented on this paper. The leadframe design is integrated with connecting bars that can be routed and bonded with wires to decrease the wire span and create a more manufacturable wirebonding structure in densified design of QFN. In addition, the connecting bars produced an inter-connection link between relocated pads and extended input/output (I/O) leads for the 3rd array electrical connections. The implementation of the proposed augmented design would improve the manufacturability of multiple arrays of I/O in QFN, enabling cost-saving initiative and manufacturing solution to devices with multiple arrays requirement.

Keywords: Leadframe design; QFN; multi-row; assembly.

1. INTRODUCTION

The introduction of densified version of Quad-Flat No-lead (QFN) packaging became the interest of Integrated Circuit (IC) manufacturer [1] since it can be an alternative solution to the transition of Ball Grid Array (BGA) devices to cheaper packaging like QFN which is anticipated

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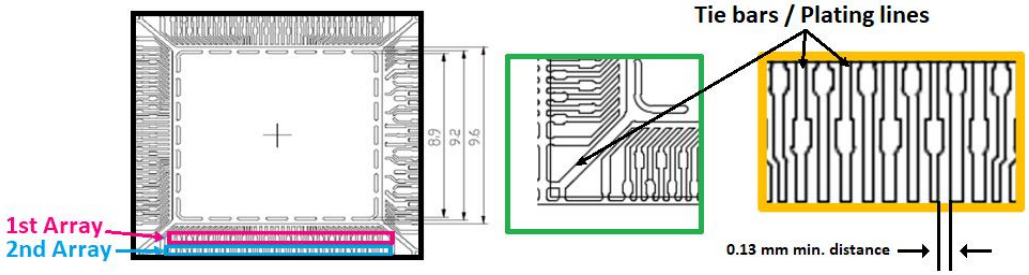

Fig. 1. QFN with dual array of I/O

to bring down the cost of the unit by more or less 50%. On the other hand, this may enable also to increase the topographies of electronic product in terms of its application and performance. However, densification became challenging for QFN devices due to the existing constraint in equipment, manufacturability and design aspect [2-5]. Current configuration for QFN shown in Fig. 1 is restricted only to one (1) or two (2) arrays of I/O interconnects wherein three (3) or more arrays of input/output (I/O), are still on premature stage. There are multiple factors found to be detractors in the implementation of multiple rows (> 2 rows). The number of I/O, in design point-of-view, that can be embedded in a particular package dimension is considering the etching capability of the leadframe supplier, thus an approximate clearance between metal to metal of minimum 0.13 mm is maintained. Incorporating the 3rd array of results to a larger package dimension wherein the required span of wire to attach the silicon bond pads to the 3rd array of I/O is longer. A longer wire span is critical in wirebonding process since it can easily induce "wire shorting" on the neighboring wire. The wire shorting issue is anticipated in densified packages with shorter distance between bond pad opening (BPO) with extended I/O location. Note that wire length and other design limitations are governed by assembly design rules [3,6-7]. In manufacturing point-of-view, longer span of wire easily sway during encapsulation process, resulting to wire shorting rejection especially on the wire adjacent to the direction of the mold flow.

The implementation of connecting bars reduces the length of the wire required between bondpads and I/O which promotes cost saving initiative for devices that uses noble metal such as Gold (Au). Shorter wire produces stable wiring structure and routing of bondpads produces robust wiring layout. Realization of this proposed design improvement creates robust design for devices with multi-row or multiple arrays of I/O requirement.

2. LITERATURE REVIEW AND PACKAGE DESIGN IMPROVEMENT

Realization of the proposal is through modification in the leadframe design which will be fabricated with connecting line and wirebonding layout improvement. Fig. 2

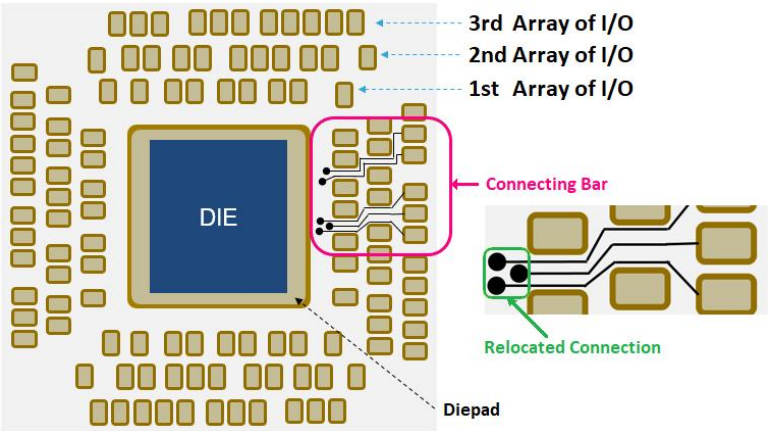

Fig. 2. QFN with relocated connection line

illustrates the proposed design wherein the connecting bar is incorporated to an etchable leadframe to produce relocated or re-layout connection pad. The identified wiring connection or I/O with high possibility of shorting wire can be relocated to other location inside the device where there is less risk of shorting wire. Usually the 3rd array of I/O has the highest possibility of shorting wire occurrence due to the long wire needed between bond pad and 3rd array of I/O.

3. RESULTS AND DISCUSSION

The connection line can be fabricated in-between I/O openings until relocated position, a wire can be attached from the bond pads of the die to the opposite end of the line or the relocated connection for inter-connection.

A connecting line between an open I/O and active I/O can be also done with this proposal. An open I/O pertains to the lead that has no required connection to the PCB board or electrical continuity between the silicon die and board. An open I/O can be intentionally fabricated inside the device instead of relocated connections line to create a junction connection to the 3rd array of I/O. Fig. 3 shows the proposed design with junction connection between silicon die and 3rd array of I/O.

A wire connection is formed through wirebonding process to create inter-connection between open I/O or relocated connection line. Wire material can be Gold or Copper (Cu) which is the recommended material currently in used for semiconductor packaging as shown in Fig. 4. Note that wirebonding requirement varies with the product and the technology [7-10].

The fabrication of the augmented design of leadframe is shown in Fig. 5. The recommended leadframe technology used in this proposal is “tapeless” leadframe since it does not require bus or plating line in the I/O layout and thermal pad or diepad. Instead of electro-plating, tapeless leadframe uses metal deposition and masking process to integrate Silver (Ag) material as coating to the I/O and diepad. As a replacement for plating line in the proposed layout, the clearances between I/O can be used to route the connecting line.

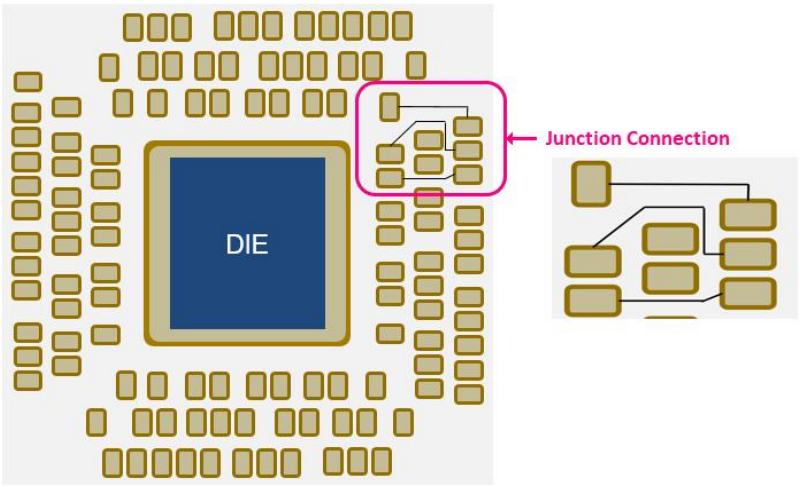

Fig. 3. QFN with junction connection

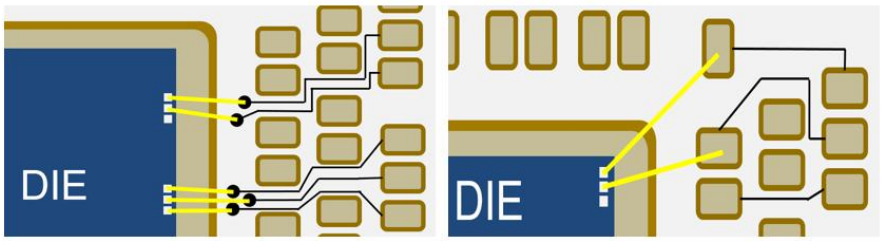

Fig. 4. Wirebonding layout

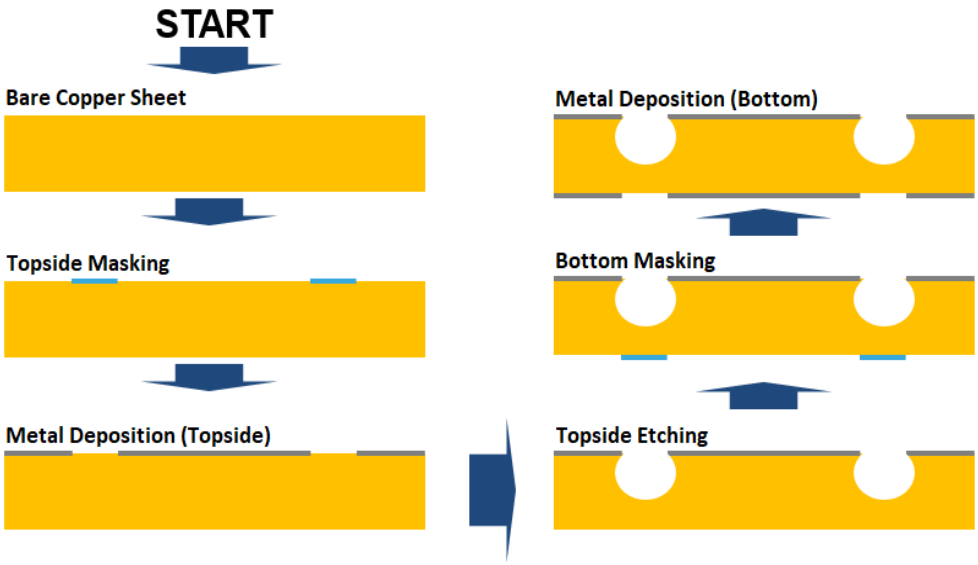

Fig. 5. Fabrication

The fabrication of connecting line in the design will be done during the topside masking and metal deposition process. A defined layout of the leadframe will be transferred to the topside portion of the bare Copper, known as masking process, with only the required portion of the Copper will be deposited with metal. On current configuration of leadframe, Silver is the suitable material used to coat the topside and bottom design of the leadframe due to its good intermetallic property with Gold and Copper which is the common wirebonding material.

This paper ultimately addressed the design and fabrication method of a QFN package with capability for high density and wiring layout solution for complex interconnection requirement. The overall objective of the proposed augmented design is to improve further the current design of a QFN to be able to adapt to the emerging new technological advancement is realized through the implementation of the proposal.

4. CONCLUSION AND RECOMMENDATIONS

The integration of connecting line in the current design layout of QFN and similar devices able to improve and provide alternative solution for complex and densified version of product. The chronic issue caused by wire shorting would be mitigated with the improved design. Prototypes are helpful for future works to validate the effectiveness of the stand-off design on tapeless leadframe device. Though the paper focused on improvement of QFN multi-row leadframe design, continuous process and design improvement is imperative to foster and sustain high quality performance of semiconductor products and its assembly manufacturing.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

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